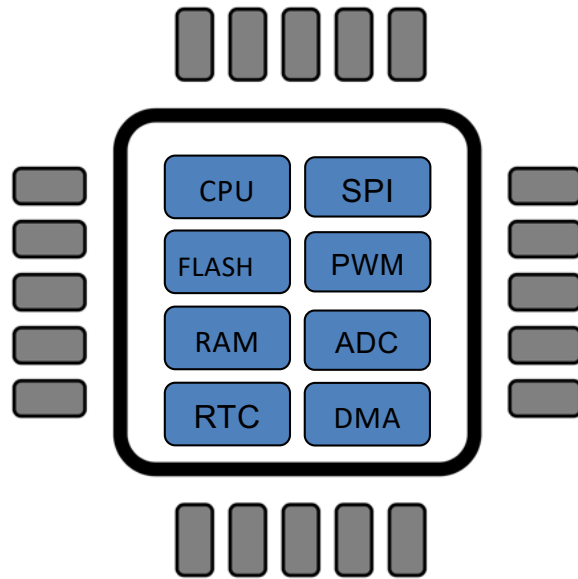


Embedded systems

Hardcore vs Softcore

Microcontrollers



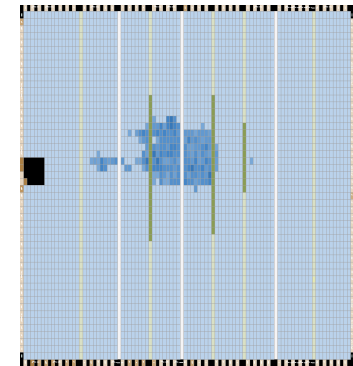
Hardcore vs Softcore

- Softcore

- Implementation defined by VHDL description
- Programming of FPGA needed to realize CPU system

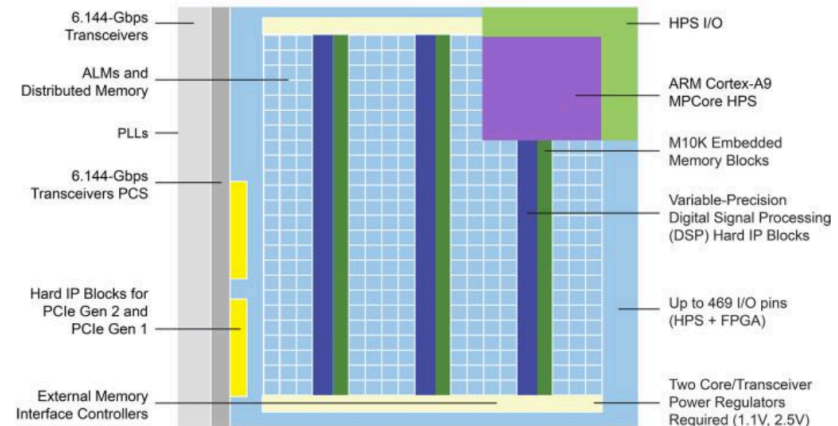
```
component nios2_system is--
  port (
    clk_clk           : in  std_logic           := 'X';           -- clk-
    i2c_avalon_mm_if_scl_export : inout std_logic           := 'X';           -- export-
    i2c_avalon_mm_if_sda_export : inout std_logic           := 'X';           -- export-
    interrupt_pio_ext_export : in  std_logic_vector(2 downto 0) := (others => 'X'); -- export-
    led_pio_ext_export : out  std_logic_vector(9 downto 0);       -- export-
    reset_reset_n      : in  std_logic           := 'X';           -- reset_n-
    sw_pio_ext_export  : in  std_logic_vector(9 downto 0) := (others => 'X'); -- export-
  );
end component nios2_system;--

u0 : component nios2_system--
  port map (
    clk_clk           => CONNECTED_TO_clk_clk,           -- clk_clk-
    i2c_avalon_mm_if_scl_export => CONNECTED_TO_i2c_avalon_mm_if_scl_export, -- i2c_avalon_mm_if_scl.export-
    i2c_avalon_mm_if_sda_export => CONNECTED_TO_i2c_avalon_mm_if_sda_export, -- i2c_avalon_mm_if_sda.export-
    interrupt_pio_ext_export => CONNECTED_TO_interrupt_pio_ext_export, -- interrupt_pio_ext.export-
    led_pio_ext_export => CONNECTED_TO_led_pio_ext_export, -- led_pio_ext.export-
    reset_reset_n      => CONNECTED_TO_reset_reset_n,    -- reset_reset_n-
    sw_pio_ext_export  => CONNECTED_TO_sw_pio_ext_export  -- sw_pio_ext.export-
  );
```



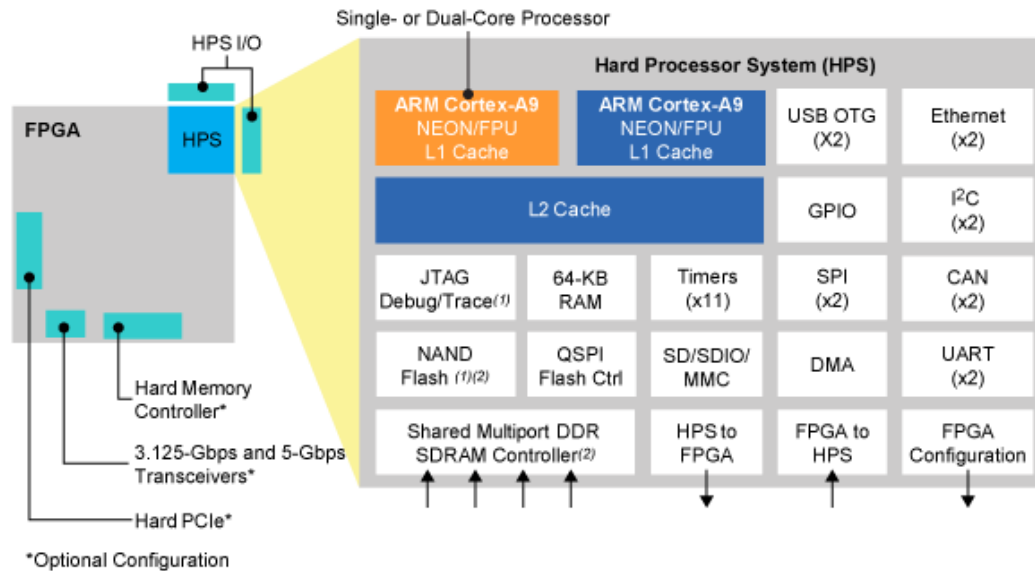
- Hardcore

- Implementation defined in silicon
- CPU system already present in silicon

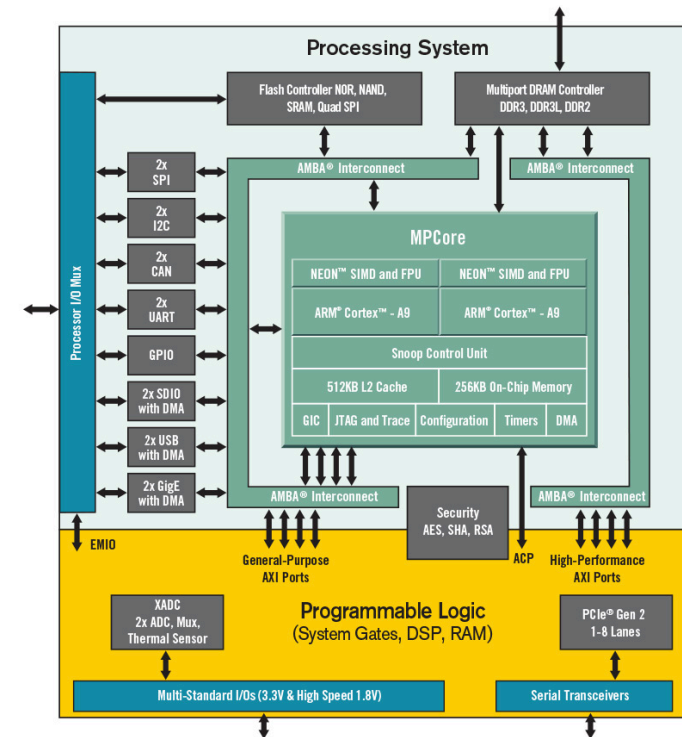


Intel Cyclone 5
Image credit: Intel.com

Example hardcore



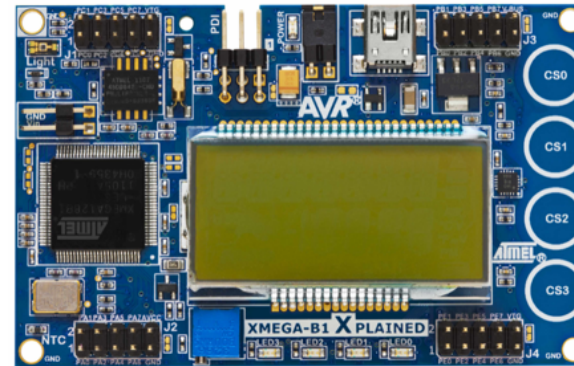
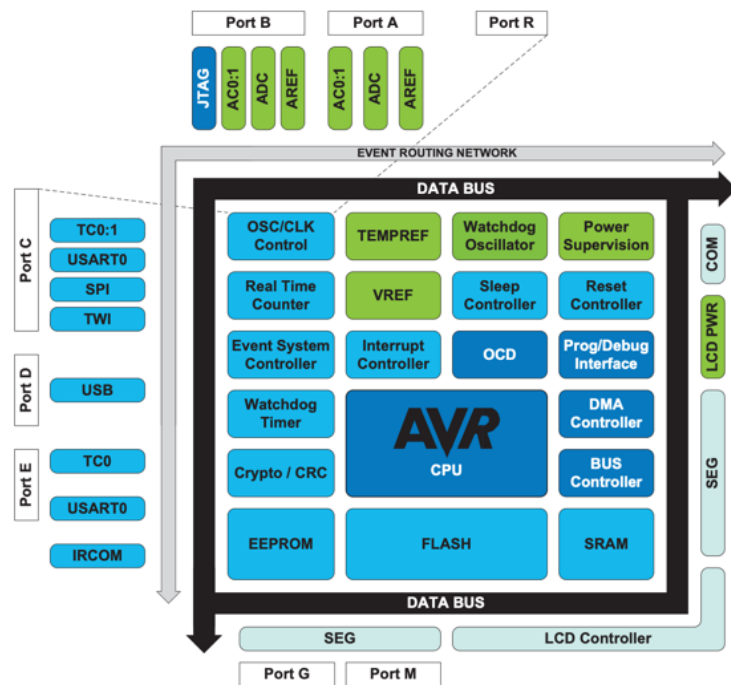
Intel Cyclone 5 SoC



Xilinx Zynq7000

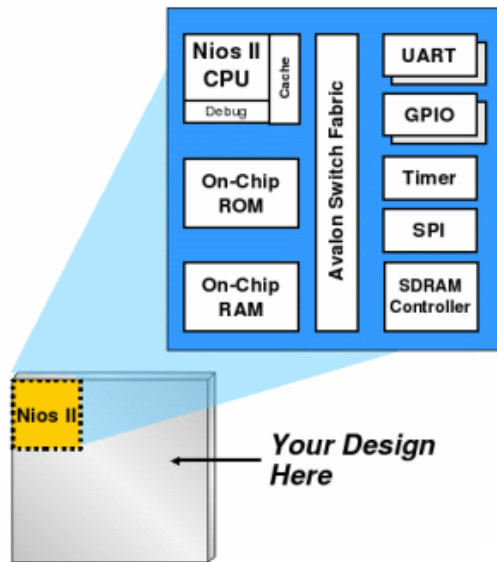
Example of hardcore (uC)

ATxmega128B1

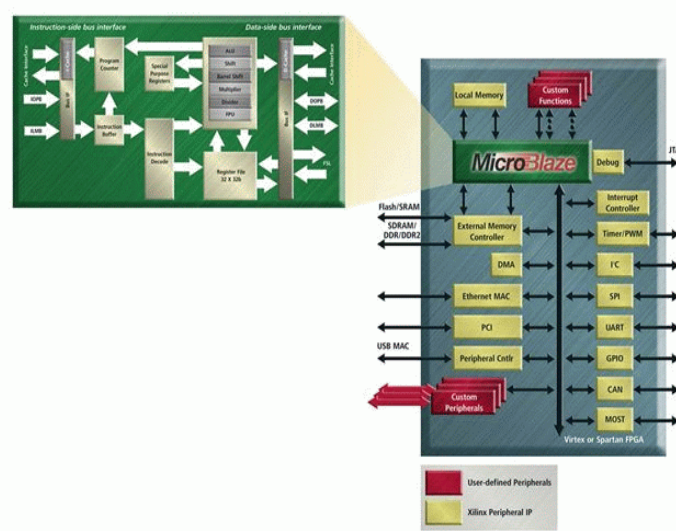


Example Softcore CPUs

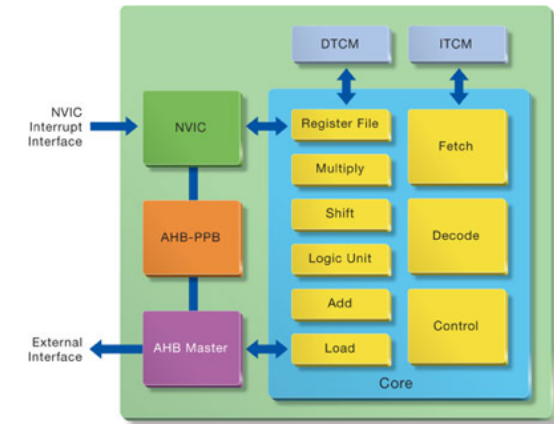
Alteras NIOS II



Xilinx microBlaze



ARM Cortex-M1

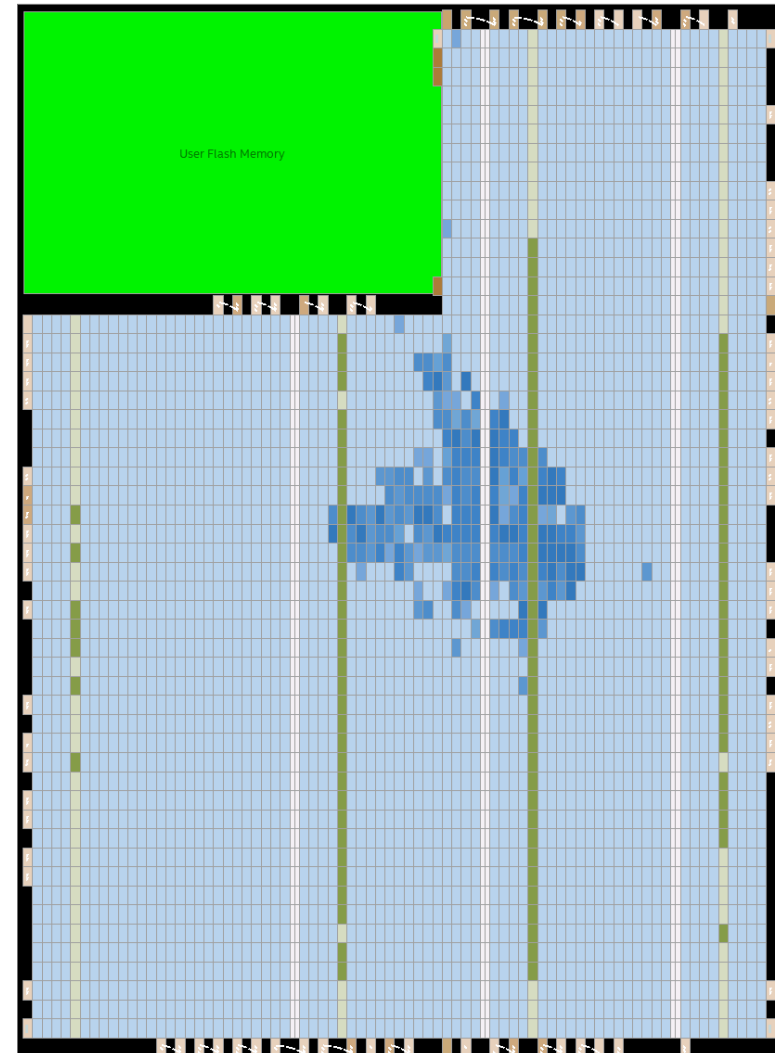
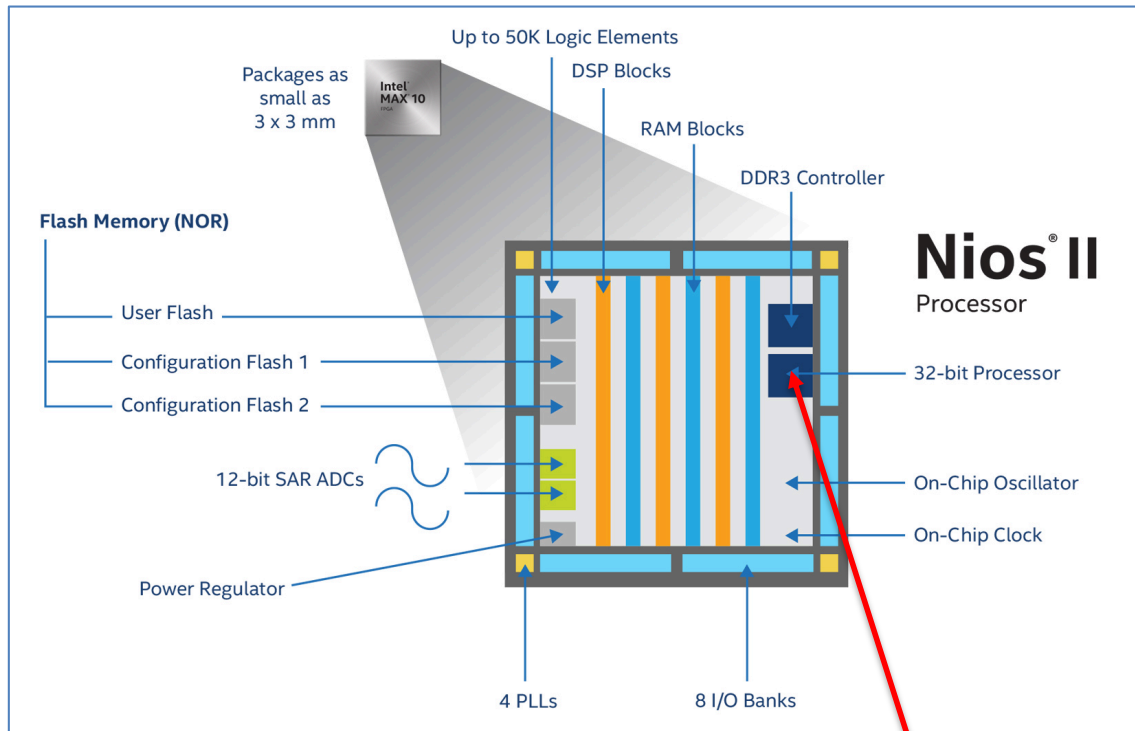


A soft core processor is a microprocessor fully described in software, usually in an HDL, which can be synthesized in programmable hardware, such as FPGAs

```
lab4_qsys_gx_1 : lab4_qsys_gx
port map (
  clk_clk           => clk,
  reset_reset_n    => areset_n,
  pio_led_external_connection_export => ledr(7 downto 0),
  i2c_wrapper_sda_export => sda,
  i2c_wrapper_scl_export => scl,
  pio_interrupt_ext_export => (alert_rr & pio_int_rr)
);
```

Example softcore

Intel MAX 10 FPGA



Softcore IPs

Soft core processor

- Pros:
 - Include the processor core only when needed
 - Include only needed features
 - The number of cores is flexible.
 - Can reuse the design in newer generations of FPGAs in the future. (Mostly vendor limited)
- Cons:
 - May be slower and simpler than hard processor cores.
 - Less area efficient compared to hard cores (Firm IP)