Total Commander 7.02a - NOT REGISTERED Súbor Označiť Príkazy Sieť Zobraziť Konfigurácia Štart Pomocník 📓 👯 🛸 🗣 🌩 🏥 🗰 🕵 🗱 🖍 📉 🍰 🎒 [-c-] 🗸 [\_žiaden\_] 161 925 944 kB z 195 358 400 kB voľné 🛝 .. [-c-] 🔽 [\_žiaden\_] 161 925 944 kB z 195 358 400 kB voľné 🛝 .. c:\varchola\--= INSTAL =--\MP7\_TOOL\_CHAIN\\*.\* c:\varchola\obr\_inst\\*.\* \* 🔻 \* 🔻 Ext Veľkosť Dátum Ext Veľkosť Dátum **↑Meno** Atrib **↑Meno** Atrib <DIR> 04.12.2007 15:48 ----<DIB> 05 12 2007 06:57 ----貪[..] <u>\_</u>€[..] instaling ACTEL TOOL.. doc 1 171 968 04.12.2007 16:14 -a--🛅 (Glue) <DIR> 04.12.2007 15:48 ----CoreConsole\_v14 zip288 505 154 05.11.2007 11:08 -a--FlashProv60SP3 exe92 666 362 05.11.2007 11:01 -a--LiberolDE80 zip632 757 145 05.11.2007 10:59 -a-ex661 189 292 05.11.2007 11:34 -a-exe82 136 688 12.11.2007 16:57 -a--🛱 SoftConsole\_v2\_0\_set.. zipi 09 487 250 05.11.2007 11:02 -a--0 kB / 1 822 990 kB v 0 / 6 súboroch, 0 / 1 priečinok(ov) 0 kB / 1 144 kB v 0 / 1 súboroch .varchola\--= INSTAL =--\MP7\_TOOL\_CHAIN> F3 / Zobraziť F4 / Upravit F5 / Kopírovať F6 / Pres. /Prem. F7 / Nový priečinok F8 / Odstrániť Alt+F4 / Skončiť

Necessary files to install Tool-chain for ACTEL MP7

Unzip LiberoIDE80.zip and run the exe file

Start by installing Libero IDE

Install Libero Gold License

InstallShield Wizard	
C Libero Platinum or E val License	
⊙ Libero Gold License	Libero
O Designer Gold, Platinum, or Eval License	Integrated Design Environment
◯ Go to Libero IDE website	
InstallShield	< <u>B</u> ack <u>N</u> ext > Cancel

Click NEXT for several times and wait to complete the installation of LIBERO.

You were been asked to choose way of installing the license at the end of installation. You have to visit actel website before the installation to request license.dat file for LIBERO IDE. This file could be downloaded from actel website or from your mailbox after requesting the LIBERO GOLD LICENCE (1 year license for using up to 1.000.000 gates). Copy this file into C:\flexlm\licence.dat. In following window choose:



And reboot your computer.

Actel Libero IDE v8.0	
	InstallShield Wizard Complete
	Setup has finished performing the requested action. Be sure you have received and properly installed your Libero IDE software license prior to use. You must restart your computer, login as an Administrator or Power User, and invoke Libero to complete the installation.
	You MUST Reboot. Do you want to do it NOW ?
	Yes, I want to restart my computer now.
	No, I will restart my computer later.
	Remove any disks from their drives, and click Finish to complete Setup.
Instalished	K Back Finish Cancel
an availantiera	

Open the System Properties Window by right-click on My Computer. Select the Advanced tab and click on the Environment Variables:

System Properties
System Restore Automatic Updates Remote
General Computer Name Hardware Advanced
You must be logged on as an Administrator to make most of these changes.
Performance
Visual effects, processor scheduling, memory usage, and virtual memory
<u>S</u> ettings
User Profiles
Desktop settings related to your logon
<u>Settings</u>
Startup and Recovery
System startup, system failure, and debugging information
Se <u>t</u> tings
Environment Variables Error Reporting
OK Cancel Apply

Create new variables: LM\_LICENCE\_FILE and SYNPLICITY\_LICENSE\_FILE with C:\flexIm\License.dat file path. File License.dat is also necessary to copy into folder: Libero/Desinger/adm/

Em	vironment Varial	bles	?×
_	Iser variables for DS	P	
		· · · · ·	
	Variable	Value	
	LM_LICENCE_FILE	- c:\flexIm\license.dat;c:\flexIm\cclicense	
	TEMP	c:\nexim\license.dat C:\Documents and Settings\DSP\Local S	
	TMP	C:\Documents and Settings\DSP\Local S	
	VCToolkitInstallDir	C:\Program_Files_Embedded\ACTEL\Lib	
		<u>N</u> ew <u>E</u> dit <u>D</u> eleti	e
L C	<u>5</u> ystem variables		
	Variable	Value	
	ComSpec	C:\WINDOWS\system32\cmd.exe	
	FP_NO_HOST_C	NO	
	NUMBER_OF_P	2 USE device NT	
	Path	C:\Program Files Embedded\ACTEL\Lib	~
	radii	ent rogram_ nos_enboddodtAeneetabrit	
		New Edit Deleti	e
		OK Car	ncel

Install the SP3 service pack for Libero 8.0 by executing LiberoIDEv80SP3.exe file. Click NEXT for several times.

Continue with installing the CoreConsole: CoreConsole\_v14.exe



Click NEXT for several times to complete the installation

You will be asked about licences again:

Setup	
2	CoreConsole requires a license in order to run. Do you want to visit the Actel License & Registration website now to obtain a license?
	Yes No

So, if you have not a license, visit ACTEL's website and request for it.

Received license rename to cclicense.dat and copy into C:\flexlm\ And into LM\_LICENCE\_FILE path in Envirionment variables.

Last stage for MP7 designing is the SofConsole. Run its installation by executing: SoftConsole\_v2\_0\_setup.exe

The alternate option of ARM software development toolkit is KEIL uVision3 IDE with RealView compiler (in demo-version up to 16kB of code) or free GNU GCC by CodeSourcery. CodeSourcery compiler is used in softconsole too, so we will make interconnection between KEIL uVision IDE and GNU GCC compiler. At first run installation of uVision3 by executing: mdk311.exe. Click several times NEXT for success installation of KEIL.

Now we prepare interconnection between KEIL and CodeSourcery GNU GCC from the SoftConsole installation by following instructions in GLUE/readme.txt At first copy all files instead readme.txt from GLUE folder into BIN folder of Sourcery G++:

💾 Total Commander 7.02a - NOT	REGISTERED					- 7 🗙
Files Mark Commands Net Show C	onfiguration Start					Help
		TTP. UNL AM D. D.D.	A   A			
	2 4 4 <b>H</b> H	88 86 MM 8% 848				
[-c-] 🗸 [_none_] 161 925 768 k of	195 358 400 k free		N	[-c-] V [_none_] 161 925 768 k of 195 358 40	D k free	N
c:\Program Files Embedded\ACTEL	SoltConsole v2.0.0.13\Soft	Console v2.0.0.13\Sourceiv	G : : \bin\*, * 🖛	c:\varchela\ - INSTAL - \MP7 TOOL CHAIN'	\Glue\*,*	* -
↑Name		Ext Size Da	ate At	↑Name	Ext	Size Date At
<u>د.</u> ]		<dir> 04</dir>	.12.2007 10:08	<u>د.</u> ]		<dir> 04.12.2007 15:48</dir>
🛐 arm-none-eabi-abiactel		dli 380 928 11	.09.2007 17:01 -a	arm-glue-ar	bat	20 20.10.2006 10:12 -a-
arm-none-eabi-addr2line		exe 453 120 24	.07.2007 20:14 -a	arm-glue-as	bat	204 27.09.2006 12:02 -a-
arm-none-eabi-ar		exe 421 888 24	.07.2007 20:14 -a	arm-glue-as	exe	20 147 09.05.2007 00:15 -a-
arm-none-eabi-as		exe //516824	.07.2007 20:14 -a	arm-glue-gcc	bat	165 27.09.2006 12:10 -a- 20 147 09 05 2007 00:15 -a
arm-none-eabi-c++filt		exe 452 096 24	07 2007 20:14 -a	arm-glue-obicon	exe	20 483 09 05 2007 12 10 -a
arm-none-eabi-cpp		exe 189 440 24	.07.2007 20:14 -a	asar gala asi asi asi asi asi asi asi asi asi as	exe	33 433 07.11.2002 20:53 -a-
arm-none-eabi-g++		exe 190 976 24	.07.2007 20:14 -a	🗊 readme	txt	1 039 14.05.2007 18:13 -a-
arm-none-eabi-gcc		exe 188 416 24	.07.2007 20:14 -a	-		
arm-none-eabi-gcc-4.2.0		exe 188 416 24	.07.2007 20:14 -a			
arm-none-eabi-gcov		exe 39 424 24	.07.2007 20:14 -a			
arm-none-eabi-gdb		exe 3 494 400 24	.07.2007 20:14 -a			
arm-none-eabi-gpror		exe 514 560 24	07.2007 20:14 -a			
arm-none-eabi-nm		exe 462 848 24	07 2007 20:14 -a			
arm-none-eabi-objcopy		exe 598 528 24	.07.2007 20:14 -a			
arm-nane-eabi-objdump		exe 717 312 24	.07.2007 20:14 -a			
in arm-none-eabi-ranlib		exe 421 888 24	.07.2007 20:14 -a			
arm-none-eabi-readelf		exe 245 248 24	N7 2007 20:14 -a-			
arm-none-eabi-run		exe 616 960 24	.07.2007 20:14 -a			
arm-none-eabl-size		exe 405 015 24	10 2007 20:14 -a			
arm-none-eabi-strings		exe 406 528 24	.07.2007 20:14 -a			
arm-none-eabi-strip		exe 598 528 24	.07.2007 20:14 -a			
cs-make		exe 165 888 24	.07.2007 20:14 -a			
CS-rm		exe 37 376 24	.07.2007 20:14 -a			
gmake		exe 164 352 28	.03.2007 11:27 -a			
No. 1		dli 369 394 28	.03.2007 11:27 -a			
таке		exe 164 352 28	.03.2007 11:27 -a			
		Total Commander				
		Lopy / niels) to				
		HALMACTEL SCHOOL				
		Discover a level of con-	SUIC V2.0.0.133501(COP	BOID V2.0 0 TSXS00100 / BTTX01X		
		Only files of this type		Options		
				~		
		ConuNTES nerroise	ions (may need adminis	trator rightst		
			F2 Queue	<u>Iree</u> Cancel		
0 k / 13 466 k in 0 / 29 files				92 k / 93 k in 7 / 8 files		
c:\varchola\=	NSTAL =\MP7_TOOL_CHA	IN\Glue>				~
F3 View	F4 Edit	F5 Copy	F6 M	ove F7 NewFolder	F8 Delete	Alt+F4 Exit
Hetart	Project Napager	Total Commandar 7.0	Lister - Johnson	pola)- El instalion ACTEL TOOL		S ( ) ( ) ( ) ( ) ( ) ( )
	C.(	- rotar commander 7.0	a cister - [c:/varu	initianity Active root		

At the second, run KEIL. Close opened project. From toolbar menu choose Project -> Manage -> Components, Environments, Books...

In Folders/Extensions tab check Use GNU Compiler

In GNU-Tool-Prefix insert arm-glue-

And browse location of GNUARM folder of CodeSourcery GNU GCC in Cygnus Folder. Click OK.

Components, Environment and Books	X		
Folders/Extensions			
Development Tool Folders			
Use Settings from TOOLS.INI:	C Source: *.c		
Tool Base Folder:	C++ Source: C++		
<u>B</u> IN:	Asm Source: .asm		
INC:	Object: .obj		
LIB:	Library: .lib		
Regfile:	Document: .txt		
Select ARM Development Tools         □       Use RealView Compiler         □       Use Keil CARM Compiler         □       Use Keil CARM Compiler         □       Use GNU Compiler         □       Use GNU Compiler         □       GNU-Tool-Prefix: Cygnus Folder:         □       CTEL\SoftConsole v2.0.0.13\Soft	Console v2.0.0.13\Sourcery-G++\		
OK Cancel Defau	ilts Help		

Close the Keil.

#### INSTALING DRIVERS FOR FLASHPRO3

Execute FlashProv60SP3.exe. Click NEXT and OK for several times. You will prompted to restart the PC.



Restart it.

After restart connect your FlashPro3 into USB.

Found New Hardware Wizard			
	Welcome to the Found New Hardware Wizard Windows will search for current and updated software by looking on your computer, on the hardware installation CD, or on the Windows Update Web site (with your permission). Read our privacy policy		
	Can Windows connect to Windows Update to search for software? Yes, this time only Yes, now and every time I connect a device No, not this time Click Next to continue.		
	< Back Next > Cancel		





Found New Hardware Wizard	
Please wait while the wizard installs the	e software
Actel FlashPro3 Firmware Loader	
CyUsb.sys To C:\WINDOWS\system32	NDRIVERS
	< <u>B</u> ack <u>N</u> ext > Cancel

Found New Hardware Wizard		
Found New Hardware Wiz	Completing the Found New Hardware Wizard The wizard has finished installing the software for: Actel FlashPro3 Firmware Loader	
	Click Finish to close the wizard.	

Found New Hardware Wizard			
	Welcome to the Found New Hardware Wizard		
	Windows will search for current and updated software by looking on your computer, on the hardware installation CD, or on the Windows Update Web site (with your permission). <u>Read our privacy policy</u>		
	Can Windows connect to Windows Update to search for software?		
	○ Yes, this time only		
	<ul> <li>Yes, now and every time I connect a device</li> <li>No, not this time</li> </ul>		
	Click Next to continue.		
	< Back Next > Cancel		

Found New Hardware Wizard		
It is wizard helps you install software for:         Actel FlashPro3 Programmer         It your hardware came with an installation CD or floppy disk, insert it now.         What do you want the wizard to do?         Install the software automatically (Recommended)         Install from a list or specific location (Advanced)         Click Next to continue.		
< <u>B</u> ack <u>N</u> ext > Cancel		

Now is your FlashPro3 ready to use.

### CREATING THE NEW PROJECT WITH CORE MP7

Run Libero IDE: start -> program files -> Actel Libero IDE v8.0 -> Project manager

Create new project -> Project -> New Project

New Project Wizard			
Welcome to the New Project Wizard This wizard creates a new Libero project.			
Start Select Device	Project <u>n</u> ame:	MP7_Tutorial	
Select Tools Add Files	Project Jocation:	C:\Actelprj\MP7_Tutorial	Browse
Finish	Preferred HDL ty	<u>pe:</u> C V <u>e</u> rilog	
		• V <u>H</u> DL	Help
	< Back	Next >	Cancel

Click NEXT

New Project Wizard				
Family, Die and Package Select the family, die and package of your new project.				
Start Select Device Select Tools Add Files Finish	Family: Fusion ▼ Die: AFS090 AFS250 AFS600 M7AFS600 M1AFS600 AFS1500	Package: 208 PQFP 256 FBGA 484 FBGA	Help	
	< Back Next >	Finish	Cancel	

Make same selections and click NEXT:

New Project Wizard				
Select Integrated Tools Select the tools you want to use with your new project.				
Start Select Device Select Tools Add Files Finish	Core Configurator Core Configurator CoreConsole Synthesis Synplify Synplify Simulation ModelSim Simulus	Add     Edit     Remove     Restore Defaults     Help		
	< Back Next >	Finish Cancel		

Select Tools, but, there is a question mark by Core Console after a new installation. So, Double click onto CoreConsole:

Edit Profile		×
Name: Select a tool integration: Version:	CoreConsole CoreConsole v1.3 or later	
Process		
Location: ? core	console.exe Browse	
Additional parameters		
Restore Defaults	Help OK Cancel	

And browse location of coreconsole.exe: ...\CoreConsole\_v1.4\bin\CoreConsole.exe, click OK. In New Project Wizard click NEXT and NEXT once again and FINISH.

Import Top.vhd, that is vhdl file of top entity, where are two entities: MP7 processor and prescaler. Global clock of FUSION is 50MHz, whilst max frequency for MP7 is only 20MHz. We make 12.5MHz clock for MP7 by dividing the global clock by 4. So you can import Top.vhd by: File -> Import Files... Browse the Top.vhd

Project Manager - C:\Actelprj\MP7_T	torialWP	7_Tutorial.prj - [Project Flow]		
🥱 Project File Edit <u>V</u> iew <u>T</u> ools <u>W</u> indow !	elp			_ 8 ×
R 🖉 🖥 🗋 🚔 🗐 X 🖬 🖻 🖄 🔊	两角	🎼 🙀 🙀 🍜 🧣 🔲 Enable Designer Block cr	creation	
Current Designer view: Impl1				
Design Explorer 4 - ×		<u>.</u>		1
Show: Components		Design Entry Tools	Root : Top	<u>^</u>
work     Top (Top.vhd)     ARM7_ESC ()     C K div4 ()	HDL	Editor SmartDesign CoreConsole	v v	Confi <u>c</u> =
		€.		
Hierarchy Files		Source Files		
		<u>+</u> ,	* Simulation	
Catalog     # * X       Name filter:     Function filter:       *     *       •     *       •     •	<	Synthesis Synplify	Simulation	■ St
+ Masic Blocks	Projec	t Flow		
<u> </u>				
Elock & Management	* Look	* Library *	Type: All Find C	options >>
Information Window	Re Re TI	eading file 'ARM7_ESC.vhd'. eading file 'Top.vhd'. he Workshop_1 project was opened he Workshop_1 project was closed he WD7_Turoiel project was crea	d. d.	
Properties 🙆	Re Re	eading file 'Top.vhd'.		
File Path: C:\Actelprj\MP7_Tutorial\hdl\Top.vhd 🗸		<b>All</b> ∧ Errors ∧ Warnings ∧ Info ∧ Find 1 /		~
Ready			VHDL FAM: Fusion DIE: M7AF5600 PKG:	484 FBGA 🏼 🎢

We create the Prescaler now: In left column of windows, select in CATALOG window Clock & Managemet -> Clock – Divided and Delayed



In opened Window make next selections:

Divided and Delayed Clock : Create Core	
Input clock source: Divider:	Qutput delay: 0.000 ns  GL
	Output delay:
	Generate Reset
Help	Close

And click Generate button. Enter name of component CLK\_div4.

Generate Core		×
<u>C</u> onfigured cores	:	
C	THE AM	_
Core <u>n</u> ame:		_
Output format:	VHDL	<b>–</b>
Additional output	:	
Resource	report	
Help	OK Cancel	

And click OK.

Be sure that a question mark infront of CLK\_div4 in Design Explorer were changed into smartgen icon:



Continue by creating your MP7 core. In Design Flow window click on the Core Console in Design Entry Tools section. In opened window enter name of component: ARM7\_ESC

New	
Select a Type: Schematic SmartDesign Component CoreConsole Component IP Component VHDL Source File Verilog Source File Stimulus Stimulus HDL File Stimulus HDL File SDC File (sdc) Physical Design Constraint File (pdc) VCD File (vcd) SAIF File (saif) VHDL Template Verilog Template	CoreConsole Component
Help	OK Cancel

And click OK and the CoreConsole will be opened.

CoreConsole - ARM7_ESC	
<u>File View Actions Options H</u> elp	
Components Generate	
Selected Component's Details	
CoreMP7 Actel's CoreMP7 is a soft IP version of the popular ARM7TDMI-S that has been optimized to maximize speed and minimize size in Actel's Flash-based FPGAs. CoreMP7 is well suited for use in a number of applications, including digital cameras, kitchen appliances, automotive traction control systems, car infotainment systems, robotics and medical equipment. Actel's Version 2.0 3 of 3 Add	
Components available for selection Listed: 40 of a total of 40 components Filter	
Processors, Actel	
Core8051s	
CoreABC	
Core429	

Choose the CoreMP7 from list Processors, Actel in the left side of your screen and click Add button. From Bus Interfaces, Actel list choose: CoreMP7Brigde, CoreAHB2APB and two buses: CoreAHBLite and CoreAPB. From Peripherals, Actel choose: CoreAhbNvm, CoreApbSram, CoreAI, CoreTimer and CoreUARTapb twice.

By Drag&Drop arange the components in next order:



It is necessaty to interconnect the peripherals, core and buses. I is very easy with Auto - Stitch function: Actions -> Auto Stitch...

Set APB Masters & Slaves as folows:

Auto Stitching 🛛 🔀
AHB:Masters
APB:Masters
CoreAHB2APB_00:APBmaster
AHB:Slaves
CoreAhbNvm_00:AHBslave
AHBmslave0
CoreAhbSram_00:AHBslave
AHBmslave1
CoreAHB2APB_00:AHBslave
AHBmslave12
APB:Slaves
CoreAI_00:APBslave
APBmslave0
CoreUARTapb_00:APBslave
APBmslave3
CoreUARTapb_01:APBslave
APBmslave5
<u> </u>
Select All/None Stitch Cancel

And be sure that all boxes are checked. Click Stitch.

To connect other signals with top level entity apply following steps:

Move your mouse cursor over CoreMP7bridge, four icons will show. Click on the leftmost CONNECT icon.

Opened window fill in following way and click CONNECT:

Connect		$\mathbf{X}$
Connection Connection Label: UJTAG From: CoreMP7Bridge_00 V From Pin(s): UJTAG V To: Top Level V To Pin(s): V Not currently connected.	Top Level The Top Level bar groups together all of the ports present at the subsystem top level. Connections between the pins of subsystem components and the top level may be made using connection labels.	

# And once again for $RV\_ICE\_If:$

Constitue	Connect		×
Connection Label: RV_ICE_IF From: CoreMP7Bridge_00 From Pin(s): RV_ICE_IF To: Top Level To Pin(s): To Pin(s): Connected. Not currently connected. Connect Disconnect OK Cancel	Connection Connection Label: RV_ICE_If From: CoreMP7Bridge_00 From Pin(s): RV_ICE_IF To: Top Level To Pin(s): Not currently connected. OK Cancel	Top Level The Top Level bar groups together all of the ports present at the subsystem top level. Connections between the pins of subsystem components and the top level may be made using connection labels.	×××

It was made UJTAG (debuging by FlashPro3 Interface) and RV\_ICE\_If interconection with top level entity by last two steps.

Move your mouse over both CoreUARTapb, click right button on the mouse and choose CHANGE VERSION. Choose 1.2 version instead 3.1.105 for both CoreUARTapb.

Apply an auto-stitch function again.

Move mouse button over CoreUARTapb which is configured as APBslave3 and click on the leftmost CONNECT buton.

Fill window as follows:

Connect			×
Connection Connection Label: From: From Pin(s): To: To Pin(s):	R5232_RX CoreUARTapb_00  rx Top Level	Top Level The Top Level bar groups together all of the ports present at the subsystem top level. Connections between the pins of subsystem components and the top level may be made using connection levels	
Not currently of	nnect Disconnect	the top level may be made using connection labels.	~~

### Click Connect button.

#### And for TX line:

Connect			×
Connection Connection Label: From: ( From Pin(s): ( To: 1 To Pin(s): Connection OK. Top Level: and C connected.	R5232_TX CoreUARTapb_00 tx Top Level CoreUARTapb_00:tx are ect Disconnect	Top Level The Top Level bar groups together all of the ports present at the subsystem top level. Connections between the pins of subsystem components and the top level may be made using connection labels.	×××
	Cancel		

Click OK.

Move mouse button over CoreUARTapb which is configured as APBslave5 and click on the leftmost CONNECT buton.



Co	onnect			$\mathbf{X}$
	Connection Connection Label:	A3PUART_RX	Top Level	ĺ
	From:	CoreUARTapb_01		
	From Pin(s):	rx 💌		
	To:	Top Level	The Top Level bar groups together all of the ports present at the subsystem top level.	
	Not currently c	onnected.	Connections between the pins of subsystem components and the top level may be made using connection labels.	~~~
		Disconnect Disconnect K Cancel		

## Click OK.

For TX line:

С	onnect			×
	Connection Connection Label: From: From Pin(s): To: To Pin(s): Not currently co	A3PUART_TX CoreUARTapb_01 tx Top Level	Top Level The Top Level bar groups together all of the ports present at the subsystem top level. Connections between the pins of subsystem components and the top level may be made using connection labels.	~~~
		nect Disconnect K Cancel		

All interconnections are done for purpose of this tutorial.

Some of CoreXYZ bocks allow to configure its properties. Move mouse cursor over CoreMP7 and click second icon – configure. Make sure of Debug is Enabled. Click OK.

Co	onfiguring CoreMP7_00
ſ	Configuration
	Component Name: CoreMP7_00
	Die: M7AFS600 💉 🖁
	Debug: Enabled 🗸
	Speed grade: -2
	CoreMP7_00: (New Connection) Connect Any:any
	CoreMP7_00:MP7_SysIf CoreMP7Bridge_00:MP7_SysIf
	OK Cancel

Move mouse cursor over CoreMP7Bridge and click second icon - configure. Make sure of Debug is RealView or FlashPro3. Click OK

C	onfiguring CoreMP7Bridge_00	
٢	Configuration	
	Component Name: CoreMP7Bridge_00	^
	Debug: RealView or FlashPro3 🔽 🖁	
	Synchronize nIRQ: No	
	Synchronize nFIQ: No	
	Device family: Fusion	
	CoreMP7Bridge_00: (New Connection) Connect Any:any	
	CoreMP7Bridge_00:AHBmaster	
	CoreMP7Bridge_00:MP7_SysIf CoreMP7_00:MP7_SysIf	
	CoreMP7Bridge_00:UJTAG Top Level:	
	CoreMP7Bridge_00:RV_ICE_If Top Level:	
	CoreMP7Bridge_00:HRESETn CoreAHBLite_00:HRESETn	
	CoreMP7Bridge_00:HRESETn CoreAHB2APB_00:HRESETn	~
	OK Cancel	

In the same way set Amount Of Internal Flash Required at 256kBytes in CoreAhbNvm. Amount of internal SRAM required set on 10kBytes in CoreAhbSram.

Click the **Configure** icon for the **CoreAl** component. Set the following in the Configuring CoreAl\_00 dialog box. Accept the default settings for all other options and click **OK**:

٠	AT0 input:	Temperature Monitor
•	AT3 input:	Temperature Monitor
•	AT4 input:	Temperature Monitor
•	AC5 input:	0V to 8V analog input
•	AT6 input:	Temperature Monitor
•	AG6 output:	Software driven 25 mA sink
•	AG7 output:	Software driven 25 mA sink
•	AT8 input:	Temperature Monitor
•	AG8 output:	Software driven 25 mA sink
•	ADC MODE control:	Fixed constant
•	ADC MODE fixed value:	12-bit
•	TVC[7:0] pins control:	Fixed constant
•	TVC[7:0] fixed value:	0

- STC[7:0] pins control: Fixed constant 23
- STC[7:0] constant: •

Click Ok.

Your MP7 system could look like:



You can observe the memory map by: View -> Memory map.

Me	mor	v M	aD

# Memory Map for ARM7\_ESC

# CoreMP7\_00

	Base Address					
	CoreAHBLite_00:NoRemap CoreAHBLite_00:SwapSlots0and1					
<u>CoreAhbNvm_00</u>	0x0000000	0x1000000				
<u>CoreAhbSram_00</u>	0x1000000 0x0000000					
<u>CoreAl_00</u>	0xc000000					
CoreUARTapb_00	0x0	0xc300000				
<u>CoreUARTapb_01</u>	0xc5000000					
<u>p</u>						

×

#### Select Generate Tab:



And click Save & Generate.

Now you can close the Core Console by File -> Exit

Note that question mark in Design Explorer changes into CoreConsole icon:

Project Manager - C:\Actelprj\MP7_T	utorial\MP7_Tutorial.prj - [Project Flow]	
🥱 Project Eile Edit View Tools <u>W</u> indow !	<u>t</u> elp	Minimize
🖪 🖉 🗖 🗖 🚔 🗐 🕺 🛍 🖻 🗠 의	: 🏘 縃 🎲 🏭 🙀 🎒 🦿 🔲 Enable Designer Block creation	
Current Designer view: Impl1		
Design Explorer 🛛 🗛 🔺 🗙		(
Show: Components	Design Entry Tools	Root : Top 🛛 🔷
work  BLACKBOX_PACKAGE (arm_syn;  Top (Top.vhd)  ARM7_ESC  CLK_div4	HDL Editor SmartDesign	> Pre-Synthe Post-Synthes Post-Layout
Hierarchy Files	Source Files	
Catalog <u> </u>	Synthesis	
Name filter:     Function filter:       *     *       A     Function, Name	Synplify new (Top.ed	Simulation ModelSim
🖃 🖼 Clock & Management		2
CCC - Dynamic	Project Flow	
Icick + Derayed           Icick + Derayed           Icick + Divided and Delayed           Icick + Divided and Delayed	Look * Librar * Type All	Find Dptions >:
Information Window	Reading file 'Tx_async.vhd'. Reading file 'Rx_sync.vhd'. Reading file 'Rx_async.vhd'. Reading file 'Clock gen.vhd'.	
	Reading file 'fifo_256x8_fusion.vhd'.	_
Properties 🥥		~
C:\Actelprj\MP7_Tutorial\hdl\Top.vhd	8 All δ Errors λ Warnings λ Info λ Find 1	>
Libeaev work		
кеаду	UVHDL FAM: Fusion DIE:	M7AF5600 PKG: 484 FBGA

The sources are complete for physical design now, it is possible to synthetize, compile, place & route and download it into flash, but first, we prepare the firmware.

There is Two Ways to create MP7 firmware Intel HEX file

- ➔ In SoftConsole
- → In Keil

We will use both ways, but, in this time (05. dec. 2007), we have under control generating the hex file in KEIL and dubuging in RAM in SoftConsole only.

Run KEIL.

Create firmware folder in your ACTEL project directory

💾 Total Commander 7.02a - NOT REGISTERED						
<u>F</u> iles <u>M</u> ark <u>⊂</u> ommar	nds <u>N</u> et Sho <u>w</u> C <u>o</u> r	nfiguration <u>S</u> tart				<u>H</u> elp
2 88 9 6	• • • • • •		) 🖨 🛛 🏭	36 🕅 📉 👯 d	3 5	
[-c-] 🗸 [_none_]	161 924 376 k of 19	95 358 400 k free	A [6	c-] 🗸 [_none_] 161 9	24 376 k of 195 3	58 400 k free 🛛 🛝
c:\Actelprj\MP7_T	utorial\*.*		* 🔻 💽	\*.*		* 🔻
↑Name	Ext	Size Date	At ↑N	Name	Ext Siz	e Date Atl
金[]		<dir> 05.12.20</dir>	107 07:45 📔	[Actel]	<di< th=""><th>R&gt; 09.11.2007 10:55</th></di<>	R> 09.11.2007 10:55
🗀 [component]		<dir> 04.12.20</dir>	107 10:21 📔	[Actelprj]	<di< th=""><th>R&gt; 04.12.2007 14:21</th></di<>	R> 04.12.2007 14:21
🗀 [constraint]		<dir> 04.12.20</dir>	107 10:21 📔	[Documents and Setti	ngs] <di< th=""><th>R&gt; 23.08.2007 20:08</th></di<>	R> 23.08.2007 20:08
Coreconsole]		<dir> 04.12.20</dir>	107 14:25 📋	] [flexlm]	<di< th=""><th>R&gt; 08.11.2007 09:55</th></di<>	R> 08.11.2007 09:55
[designer]		<dir> 04.12.20</dir>	07 10:21	[Images]	<di< th=""><th>R&gt; 28.09.2007 11:21</th></di<>	R> 28.09.2007 11:21
[firmware]		<dir> 05.12.20</dir>	107 07:45	[Program Files]	<di< th=""><th>R&gt; 04.12.2007 16:16 r</th></di<>	R> 04.12.2007 16:16 r
[hdl]		<dir> 04.12.20</dir>	107 10:25 📋	Program_Files_Embe	ddedj <di< th=""><th>H&gt; U4.12.2UU7 15:49</th></di<>	H> U4.12.2UU7 15:49
[package]		<dir> 05.12.20</dir>	107 06:57	[staff]	<di< th=""><th>R&gt; 23.08.2007 18:13</th></di<>	R> 23.08.2007 18:13
[phy_synthesis]		(DIR) 04.12.20	107 10:21	j[SynLM]	<ui (D)</ui 	R> 04.12.2007 09:32
[simulation]		(DIR) 05.12.20	07 06:57	j (varcholaj Budiki Dovući		R> 04.12.2007 08:38 D> 05.13.2007 06:34
smartgenj		(DID) 03.12.20	07 06:37	JIWINDUWSJ		0.00.09.2007.14:45
[sumbasis]		ZDIRX 04.12.20	07 10.21	CONFIG	CYC	0 06.08.2007 14.43 -a-
[synthesis]		ZDIRS 05 12 20	07 16:57	ki2log	log	2 04 12 2007 09-31
MP7 Tutorial	pri	18 203 05 12 20	107 06:57 -a	KIZIOG	iog	2 04.12.2001 03.31 0
	Pi	10 203 03.12.20	01 00.51 -0			
0 k / 17 k in 0 / 1 l	files, 0 / 13 dir(s)		01	k / 0 k in 0 / 3 files, 0	/ 11 dir(s)	
	c:\Actelprj\MP7_T	utorial>				*
F3 View	F4 Edit	F5 Сору	F6 Move	e F7 NewFolde	r F8 Delet	e Alt+F4 Exit

Open firmware directory and make subdirectories KEIL and SoftConsole in it.

Copy the source files (.c .h .ld .s) into KEIL subdirectory:

💾 Total Commander 7.02a - NOT REGISTERED						_ 2 🛛
Files Mark Commands Net Show Configuration Start						Help
2 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	🕅 📉 💱	t 🗊 🕒				
[-c-] V [_none_] 161 924 116 k of 195 358 400 k free		1	[-c-] V [_none_]	161 924 116 k of 19	5 358 400 k free	V
c:\Actelprj\MP7_Tutorial\firmware\KEIL\*.*		*	= c:\varchela\ = I	ISTAL - VACTEL MP	7 files\MP7 source\*.*	* 🕶
↑Name Ex	t Size	Date	At Name		↑Ext	Size Date At
<b>≜</b> []	<dir></dir>	05.12.2007 07:4	7 🟦 []			<dir> 05.12.2007 07:49</dir>
			core_gpio		C	1 822 22.03.2007 23:57 -a- 5 179 19 03 2007 22:17 -a-
			Coreai		c	17 974 24.11.2007 15:01 -a-
			esc07		c	8 117 01.12.2007 12:06 -a-
			uscr_ip		c	13 221 19.03.2007 22:17 a
			acm defines		c h	3 243 26 03 2007 22.17 -a-
			🕒 core_gpio		ĥ	728 22.03.2007 23:58 -a-
			core_uart_apt	i	h	1 261 19.03.2007 22:17 -a-
			Coreai		h	5 606 19.03.2007 22:17 -a-
			Coreal_regs		n b	7 415 19.03.2007 22:17 -a- 489 22 03 2007 23:58 -a-
			coreuartapb_r	egs	ĥ	1 570 19.03.2007 22:17 -a-
			📄 cpu_types		h	413 19.03.2007 22:17 -a-
			hw_macros		h	3 707 19.03.2007 22:17 -a-
			guads acm c	a	h	1 650 26 03 2007 07:43 -a-
			user_ip	3	ĥ	515 19.03.2007 22:17 -a-
			🕒 utility		h	367 19 03 2007 22-17 -a-
			debug_in_ram		ld	2 184 19.03.2007 22:17 -a-
			Crt0		2	4 382 19.03.2007 22:17 -a-
			vectors		s	840 19.03.2007 22:17 -a
	Total Comma	nder				
	Copy 23 file(s) to	)				
	c:\Actelprj\MP7	7_Tutorial\firm.ware\K	EILV:*			
	Only liles of this	type:		<u>O</u> ption:		
				~		
	Copy NTFS p	permissions (may nee	d administrator rights)			
	ОК	F2 <u>Q</u> uei	leilee	Cancel		
0 k / 0 k in 0 / 0 files			83 k / 83 k in 23	/ 23 files		
c:\varchola\= INSTAL =\ACTEL MP7 files\MP7 source>	·					✓
F3 View F4 Edit	F5 Copy		F6 Move	F7 NewFolder	F8 Delete	Alt+F4 Exit
🛃 Start 👘 🧭 🥹 🧭 🐣 💊 Project Manage 💾 Total Cor	nmand 🔽 L	ister - [c:\varz	🔚 Lister - [c:\varc	Lister - [c:\varc	👜 instaing ACTEL 🛛 🕎 mp7_fim	ware SK 🔇 🚺 🥦 7:49

In Keil toolbar menu choose Project -> New uVision Project

Create New Pro	ject				? 🛛
Savejn:	C KEIL		•	🗢 🗈 💣 📰 •	
My Recent Documents Desktop					
My Documents					
My Computer					
My Network Places	File <u>n</u> ame:	MP7_firmware		•	<u>S</u> ave
11000	Save as <u>t</u> ype:	Project Files (*.uv2)		•	Cancel

Enter name of new project (MP7\_firmware) and save it in ...\your\_actel\_project\firmware\KEIL

Next you will be promt to choose device. In latest version of KEIL (05. dec. 2007) there is no option of MP7, so, you could to choose ARM -> ARM7 (Little Endian)

Select Device for Target 'Target 1'
CPU Vendor: ARM Device: ARM7 (Little Endian) Toolset: ARM
Data base       Description:         Acroflex UTMC       Altium         Altium       Analog Devices         Analog Devices       AnchorChips         ARM7 (Big Endian)       ARM7 (Little Endian)         ARM966E-S (Big Endian)       ARM966E-S (Big Endian)         ARM956E-S (Little Endian)       ARM956E-S (Little Endian)         ARM95E-S (Little Endian)       ARM95E-S (Little Endian)         ARM95E-S (Little Endian)       ARM95E-S (Little Endian)         Cortex-M1       Cortex-M3
OK Cancel Help

Click OK.

You will see:

MP7_firmware - µVision3	
Elle Edit View Project Debug Flash Peripherals Tools SVCS Window Help	
12 ☞ 및 Ø ↓ ℡ ଈ   그 그   非 非 ル % % % 嘛	
🗇 🕮 🐲 者 🛱 🛣 Target 1 🔽 🛃 🚍	
Project Workspace × x	
Target 1 Source Group 1	
put Window ×	•
δ K K → M Build ∧ Command ∧ Find in Files /	
Ready Simulation	

Now we prepare file structure in Project Workspace window. Click twice slowly (not double-click) on Source Group1 to rename it. Enter new name: Sources. Right click on Target 1 and choose New Group and name this group Headers. Make further two groups "Linker Scripts" and "Start Up".

₩ MP7_firmware - µVision3			
File Edit View Project Debug Flash Peripherals Tools St	CS <u>W</u> indow <u>H</u> elp		
徻 🚅 🖬 🕼 👗 🖻 🛍   ユ 오   卓 卓 ル 🎗	名或 🙀		🔤 🔼 🕘 🏀 🕅 🛅
🕸 🎬 🥔 👗 🙀 🌠 Target 1			
Project Workspace 🔹 🗙			
Sources     Headers     Linker Scripts     Start Up			
x hut Mindow			
Build A Command A Find in Files /			
Ready		Simulation	

With double click on each you can add files. Add to: Sources group all .c files Headers group all .h files Linker Scripts group all .ld files Start Up group all .s files

You will be promt about file type for .ld files, choose Text Documentation:

Get Filetype for 'debug_in_ram.ld'	? 🗙
File:	<u>0</u> K
.\debug_in_ram.ld	<u>C</u> ancel
Type: Text Document file	

So now you could see:

WP7_firmware - µVision3	
Eile Edit View Project Debug Flash Peripherals Tools SVCS Window Help	
🏙 😂 🖬 🕼 🕼 🖴 🕮 卓 卓 淳 永 浅 浅 浅 🙀 📃 🔜 西	
🗇 🕮 🐲 🔏 💥 💉 Target 1 💽 🛔 🐂	
Project Workspace 🔹 👻	
Sources   Image: 1   Image: 2   Image: 3   Image: 4   Image:	
ut Window	
Build (Command ) Find in Files /	
Ready	Simulation

Keil provides option to create more "Targets" with various settings e.g. for Debuging in RAM or Run from FLASH settings. We create two targets instead Target 1: debug\_in\_ram and run\_from\_nvm according to names of linker scripts. Choose from Toolbar menu: Project -> Manage -> Environments, Components, Books...

Choose from Toolbar menu: Project -> Manage -> Environments, Components, Books... Select Project Components Tab

You will see:

Components, Environment and Bo	iks	
Project Components Folders/Extensions	Books	
Project Targets: 🛛 🗙 🗲 🗲	<u>G</u> roups: ∑ ★ ★ <u>F</u> iles	s: 🗙 🗲 🗲
Target 1	Sources Headers Linker Scripts Start Up Up	ty.c e_gpio.c e_uart_apb.c eai.c :07.c :r_io.c
Set as Current Target		Add Files
	OK Cancel Defaults	Help

In Project Targets, double click on Target 1 to rename it into Debug in RAM. Then click onto leftmost icon: new(insert) to create new Target: Run from NVM.

Components, Environment and Boo	oks 🔰
Project Components Folders/Extensions	Books
Project Targets: 🖄 🗙 🗲 Debug in RAM	Groups: ∑ ★ ↓ Files: ★ ↓ ↓ Sources Unader
	Linker Scripts core_uart_apb.c Start Up coreai.c esc07.c user_io.c
<u>S</u> et as Current Target	Add Files
	OK Cancel Defaults Help

Click OK.

Now, set make the same settings for Debug in RAM: Project -> Options for Target "Debug in RAM"

Options for Target 'Debug in RAM'
Device Target Output Listing User CC Assembler Linker Debug Utilities
Database: Generic CPU Data Base 🗾
Vendor: ARM
Device: ARM7 (Little Endian)
Toolset: ARM
Aeroflex UTMC Altium Analog Devices AnchorChips ARM7 (Big Endian) ARM7 (Little Endian) ARM966E-S (Big Endia ARM966E-S (Little Endian) ARM96E-S (Little Endian) ARM95-S (Big Endian) ARM95-S (Little Endian) Cortex-M1 Cortex-M3 ASIX Electronics Corporativ
OK Cancel Defaults Help

Options for Target 'Debug in RAM'
Device Target Output Listing User CC Assembler Linker Debug Utilities
ARM ARM7 (Little Endian)
⊠tal (MHz): 12.5
Operating system: None
OK Cancel Defaults Help

Options for Target 'Debug in RAM'	×
Device Target Output Listing User CC Assembler Linker Debug Utilities	
Select Folder for Objects <u>Name of Executable</u> : MP7_firmware	
<ul> <li>Create Executable: .\MP7_firmware</li> <li>Debug Information</li> <li>Create HEX File</li> <li>Big Endian</li> </ul>	Create Batch File
C Create Library: .\libMP7_firmware.a	
OK Cancel Defaults	Help

Options for T	arget 'Debug in RAM'	×
Device   Targ	et Output Listing User CC Assembler Linker Debug Utilities	
	✓ Do not use Standard System Startup Files     Data Start:       ✓ Do not use Standard System Libraries     BSS Start:       ✓ Use Math Libraries     BSS Start:	
Linker <u>S</u> cript File: Include Lib <u>r</u> aries	.\debug_in_ram.ld	
Include Paths		
<u>M</u> isc controls		
Linker control string	-mthumb-interwork -WI -o MP7_firmware.elf *.o -nostartfiles -nodefaultlibs	
	OK Cancel Defaults Help	

Options for Target 'Debug in RAM'	$\mathbf{X}$
Device       Target       Output       Listing       User       CC       Assemb         Image: Settings       Image: Settings       Settings         Image: Limit Speed to Real-Time       Image: Settings	ler Linker Debug Utilities C∐se: ULINK ARM Debugger ▼ Settings
✓ Load Application at Startup ✓ Run to main() Initialization File:	Load Application at Startup     Run to main() Initialization File:
Restore Debug Session Settings Breakpoints Toolbox Watchpoints & PA Memory Display	Restore Debug Session Settings Breakpoints Watchpoints Memory Display
CPU DLL: Parameter:	Driver DLL: Parameter:
Dialog DLL: Parameter: DARMP.DLL	Dialog DLL: Parameter: TARMP.DLL
OK Ca	ncel Defaults Help

Make the same settings for Run from NVM, instead Linker, where browse the . \run\_from\_nvm.ld

Options for T	arget 'Run from NVM'	×
Device Targ	et Output Listing User CC Assembler Linker Debug Utilities	
	Image: Start Start       Image: Start Start         Image: Start Start Start       Image: Start Start         Image: Start Start Start Start Start       Image: Start Start Start         Image: Start	
Linker <u>S</u> cript File: Include Lib <u>r</u> aries	<u>E</u> dit	
<u>I</u> nclude Paths		
<u>M</u> isc controls		
Linker control string	-mthumb-interwork -WI -o MP7_firmware.elf  *.o -nostartfiles -nodefaultlibs	
	OK Cancel Defaults Help	

Build the project by: Project -> Rebuild all target files...

Asigning the Intel HEX file into Libero project:

In LIBERO Catalog expand the Fusion peripherals and choose the Flash Memory System Builder.



You will see:

Flash Memory System: C	reate core									X
9 C 🛛 🗙										
Available client types		Clients used in the Flash Memory System								
Analog System				Start	Word	Pa	ge	Initiali	zation	Lock Start
Initialization Data Storage		Client Type	Client Name	Address (hex)	(hex) Size	Start	End	Order	Cost	Address
RAM Initialization				,		,		,		
ICI I Data										
Add to System										
Pipelined Bead										
		1								Countra
	Uptimize								_	<u>u</u> enerate
Help										Close
<u>.</u>									_	
Ready										

Click on the Data Storage

and full the dialogue window as follows:

Add Data Storage C	ient 🔀
Client <u>n</u> ame:	MP7_FIRMWARE
Start <u>a</u> ddress:	0 (hexadecimal only)
Size of word:	8 💌 bits
N <u>u</u> mber of words:	8192
Memory content file:	C:\Actelprj\MP7_Tutorial\firmware\KEIL\MP7_firmware.hex
Format of memory <u>c</u> on	tent file: Intel-Hex
JTAG Protection	
Prevent rea <u>d</u>	Prevent <u>w</u> rite
Help	OK Cancel

Into Memory content file browse the .hex file, which was generated by KEIL.

Click OK.

Flash Memory System: C	reate core*								
<b>9</b> ~ <b>X</b>									
Available client types		Clien	ts used in the l	Flash Memo	iry System				
Analog System	Client Type	Client Name	Start Address	Word	Pa	ge	Initiali	zation	Lock Start
Initialization	cilent Type		(hex)	Size	Start	End	Order	Cost	Address
RAM Initialization	1 🚺 Data Storage	MP7_FIRM/VARE	0	8	0	63	N/A	N/A	
CFI Data									
Add to System									
🥅 Pipelined Read									
	<u>O</u> ptimize								<u>G</u> enerate
Help									Close
Boodu									
Ready									

Click genrate.

Generate Core		
Configured cores: ARM7_ESC CLK_div4 MP7_FIRMWARE		
, Core <u>n</u> ame:	MP7_FIRMWARE	
Output format:	VHDL	Y
Help	ОК	Cancel

Write Core name and click OK

Click Close

Now you can see in LIBERO Design Explorer MP7\_FIRMWARE component:



Click on the Synthesis button. The Synplify starts:

Synplify 8.8A1 - Apr 16 2007 - [C:\Actelprj\MP7_Tutorial\syntheta)	hesis\Top_syn.prj]			
Eile Edit View Project Run Analysis HDL-Analyst Options Window Te	ch- <u>S</u> upport We <u>b H</u> elp			_ & ×
P 🛍 🗐 🎟 📴 🖬 🎒 🐇 🖻 🖻 으으 🛛 🛤 💭 😁 🗍 🕀	• Ð   ⊠ \$ 🖬   ¥	\$ \$\$ ← →	, , , , , , , , , , , , , , , , , , ,	8 11 4 1 <b> </b> E 91   k
Synplify®		1 -		Synplicity <sup>*</sup>
Add C:\Actelpri\MP7_Tutorial\synthesis	synthesis	Type log	Modified 19:26:48 0F	Simply Better Results
Change Edit		iog	13.25.46 U	Frequency (MHz) 100 Symbolic FSM Compiler Resource Sharing
Result File				I
Change Top.edn				
Target Change Actel Fusion : M7AFS600 : -1, run_prop_extract, max	fan: 12, globalthreshol	l: 50,		
RUN View Log Cancel	a <b>dy</b>			
📑 Top_syn.prj				

Click RUN button to synthetize your design

After synthetize the should not be any errors. Some warnings are OK...

Synthetize icon in Libero should be green:



Now continue with Place and route. Click on this icon:



Make sure that you will see:

Organize Constraints for Designer
Click to select a constraint file in the project, and use the Add button to pass the file to 'designer\impl1\Top.adb'. Use the Remove button to remove constraint files from Designer. Use the Up/Down arrow buttons to specify the order of the constraint files in Designer.
Constraints files in the project:       Origin         Add →          Emove
Designer only supports sdc and pdc as source files.          Image: Show this dialog before creating a new adb.         Image: Help       OK

Desinger starts... Proceed with these settings:

Device Selection Wizard		
Eamily: Fusion Die AFS090 AFS250 AFS600 M1AFS600 AFS1500	Package 208 PQFP 256 FBGA 484 FBGA	
Speed:	Die voltage:	
Cancel < <u>B</u> ack	<u>N</u> ext >	Help

Device Selection Wizard - Variations	×
Reserve Pins	
Reserve JTAG	
Reserve JIAG test reset	
Reserve probe	
L/D Attributes	
Default I/O standard:	
Please use the I/O Attribute Editor or	
PinEditor to change individual I/O attributes.	
Cancel < <u>B</u> ack <u>N</u> ext>	Help

Device Selection Wizar	d - Operating C	Conditions	X
_Junction Temperature (	in degrees Celsius)		
<u>R</u> ange:	Best:	<u>T</u> ypical:	Worst:
СОМ	0	25	70
Voltage (in volts)			
R <u>a</u> nge:	B <u>e</u> st:	Typical:	W <u>o</u> rst:
СОМ 💌	1.575	1.5	1.425
	[/O best:	I/O typical:	1/0 wor <u>s</u> t:
	0	0	0
Cancel < <u>B</u> a	ick Finish		Help

Desinger:

🏶 Designer - [Top]
B     Eile     View     Lools     Options     Help
Design Flow
Image: Compile       Image
MultiView NavigatorSmartTime Metlist Netlist Viewer PinEditor ChipPlanner ChipPlanne
The Import command succeeded ( 00:00:08 ) Design saved to file Top.adb. The Execute Script command succeeded ( 00:01:16 ) Checking for software updates Info: This software version is up to date. There are no available up
Ready FAM: Fusion DIE: M7AF5600 PKG: 484 FBGA

I tis necessary to import pin assignment file. Copy the Top.pdc file into Constraint folder. By File -> Import Source Files:

Im	oort Source Files			×
No W Us	ote: the relative order of the same type of files is im hen importing multiple EDIF or VHDL files, the top te the Up and Down buttons to specify the relative	portant. level file must be last (at the order of the files.	bottom).	
Г	Source Files		Туре	Add
1	C:\Actelprj\MP7_Tutorial\synthesis\Top.ed	In ed	in	
2	C:\Actelprj\MP7_Tutorial\coreconsole\cor	mon\A7S\M7AFS600-2\ cd	dk	Modify
3	C: VActelprjWP7_Tutorial\synthesis\Top_s	dc.sdc sd	lc	
4				Delete
5				Constant
7				Copy locally
8				+
9				<u> </u>
1	0			↓
	Merge PDC file(s) with existing physical constrain	its		
M	Merge SDC file(s) with existing timing constraints			
Au	udit timestamp: Wed Dec 05 19:33:	08 2007	Audit options	
	Help		ОК	Cancel

Click Add button and browse the Top.pdc file. Then two times the OK button. Hit Compile button. In dialogue window click OK. If everything is OK, Compile button colors green. Click on layout button and accept the default settings.

H Designer - [Top*]	
🐻 File View Iools Options Help	_ 8 ×
DG∎? TRO® → x + 0 = 3 & 9	
Design Flow	
Image: Compile       Image	]
MultiView Navigator SmartTime	
Netlist Viewer PinEditor Netlist	Smart Power
0-0-0-0-0	~
Loading the Timing data for the design. Finished loading the Timing data. TIMER: Max delay timing requirements have been met. The Layout command succeeded ( 00:03:48 )	
	>
Ready FAM: Fusion DIE: M7AF5600 PKG: 48	34 FBGA

Create programming file with click on Programming File

#### Make selections:

FlashPoint - Program	ning File	Generator - Ste	ep 1 of 1					
Silicon feature(s)	to be progra	mmed:						
🔽 FPGA An	FPGA Array							
🗌 FlashROI	м							
FlashRC	)M configura	tion file:						
				Brow	vse,			
Embedded	Flash Memor	y Blocks (EFMB):						
	Program	Block Name	Block Location	Original Configuration File				
1 🚹	<b>N</b>	ARM7_inst/CoreA	1		Modify			
I/O state during p	programming	Tri-State		•				
Help				Back Next Fin	nish Cancel			

And click on the modify button

Then	on	the	Imr	ort	configu	ration	file:
1 11011	011		1111	.010	eoning a	1401011	

Mod	Aodify Embedded Flash Memory Block									
Bloc	Block name: ARM7_inst/CoreAhbNvm_00/CoreAhbNvm_IOIL									
Bloc	k location		1							
Block configuration file: C:\Actelprj\MP7_Tutorial\smartgen\MP7_FIRMWARE\MP7_FIRMW. [Import Configuration File]										
Bloc	k content	:								
		Select All Cli	ents Unse	elect All Clients						
		Brogram	Client Turne	Client Home	Start	Client	JTAG Pr	otection	Original Momony Contant File	
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	ļ									
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And browse the location ... \project\_dir \smartgen \MP7\_FIMWARE \MP7\_FIRMWARE.efc

Click finish and name flash configuration file as fpga\_flash\_nvm\_flash

And check stapl file:

Save As					? 🔀
Save in:	impl1		•	+ 🗈 💣 🎟 -	
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1 1003	Save as type(s):	✓ Programming Data (.pdb)		STA <u>P</u> L (.stp)	Cancel

Click Save

In desinger Save project and exit it

Now, you will download the configuration file into Fusion device. Run the programming with FlashPro

Create new project

New Project	X
Project <u>N</u> ame: Programmer	
Project Location: C:\Actelprj\MP7_Tutorial\designer'	Browse
Programming mode     Single device     Chain	
OK Cancel	Help

Click OK.

Click Configure device



And Browse programming file:

Load Programm	ning File	? 🗙
Look jn:	🗁 impl1 💽 🔶 🖆 🎫 -	
My Recent Documents Desktop	Programmer isimulation Top.dtf fpga_flash_nvm_flash.stp	
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My Network Places	File name:     [fpga_flash_nvm_flash]	<u>O</u> pen
	Files of type:     All Programming Files (*.pdb; *.stp)	Cancel

Click OK.

🕼 FlashPro - [Programmer] *
Ele Edit View Iools Programmers Configuration Customize Help
New Project       Configure Device       Project         Open Project       Image: Configure Device       Image: Configure Device       Image: Configure Device         View Programmers       View Programmers       Image: Configure Device       Image: Configure Device       Image: Configure Device       Image: Configure Device
Programming file fpga_flash_nvm_flash.stp Browse Programming file information: DATE_MODIFIED Wed Dec 05 19:49:09 2007 STAPL_FILE_NAME C:\Actelprj\MP7_Tutorial\designer\impll\f CREATOR Designer Version: 0.0.4.1 DEVICE MYAFSGO0 PACKAGE MYAFSGO0-FG494 DATE 2007/12/05 STAPL_VERSION JESD71 DESIGN Top CHECKSUM 6791 SECURITY ENCRYPT FROM CORE NVM_1 ALC_VERSION 15 SILSIG 00000000 NAX_FEEQ 20000000 Chain Parameter PDB Configuration
<pre>programmer '04404' : FlashPro3 Created new project 'C:\Actelprj\MP7_Tutorial\designer\impl1\Programmer\Programmer.pro' STAPL file 'C:\Actelprj\MP7_Tutorial\designer\impl1\fpga_flash_nvm_flash.stp' has been loaded successfully. DESIGN : Top; CHECKSUM : 6781; ALG_VERSION : 15</pre>
Ready C:\Actelprj\MP7_Tutorial\designer\imp11{pga_flash_nvm_flash.stp  SINGLE

Click Program.