Freescale Semiconductor
Device Errata

Document Number: MCF52235DE
Rev. 1, 11/2006

MCF52235 Device Errata

Supports: MCF52230, MCF52231, MCF52233, MCF52234, and MCF52235

This document identifies implementation differences between the MCF52235 microcontroller and the description contained in the *MCF52235 ColdFire® Microcontroller Reference Manual*. Refer to http://freescale.com/coldfire for the latest updates. The errata items listed in this document (summarized in Table 1) describe differences from the following documents:

- MCF52235 ColdFire® Integrated Microcontroller Reference Manual
- ColdFire Microprocessor Family Programmer's Reference Manual

Table of Contents

freescale™ semiconductor

Table 1. Summary of MCF5223x Errata

Errata ID	Module Affected	Date Errata Added	Device Affected	Errata Title
1	Clock	29-Apr-2005	MCF52230 MCF52231 MCF52233 MCF52234 MCF52235	EPHY Not Accepting Valid LTP Greater Than 100 ns
2	Flash	17-Nov-2006	MCF52230 MCF52231 MCF52233 MCF52234 MCF52235	Internal Flash Speculation Address Qualification Incomplete

1 EPHY Not Accepting Valid LTP Greater Than 100 ns

1.1 Description

If a link partner's LTP is greater than 100 ns, using auto-negotiation, the EPHY does not recognize it. This results in a failure to auto-negotiate.

1.2 Workaround

Disable auto-negotiation and configure the EPHY or link partner to operate in 100TX or 10BaseT mode.

Software implementation is available in the ColdFire_Lite stack, which is available at http://www.freescale.com/coldfire.

2 Internal Flash Speculation Address Qualification Incomplete

2.1 Description

The flash controller uses a variety of advanced techniques, including two-way 32-bit bank interleaving and address speculation, to improve performance. An issue involving a complex series of interactions between the processor's local RAM (SRAM) and the local flash controller has been uncovered. In rare instances, the interaction between operand reads and writes to the SRAM and instruction fetches from the flash can result in incorrect data usage for a flash read operation. This may produce unexpected exceptions, incorrect execution, or silent data corruption.

The failing scenario includes the following:

1. A processor write to the local SRAM occurs at cycle *i*.
2. On the next cycle (cycle *i+1*), a processor read to the SRAM produces a 1-cycle read-after-write pipeline stall.
3. On the same cycle (cycle *i+1*), incorrect read data is selected for the flash access if both of the following situations occur:
   — There is a speculative flash access underway
   — The flash address and the SRAM read address have identical modulo-(flash_size) values

For example, on a device with a 256 Kbyte flash size, if flash_addr[17:0] equals sram_addr[17:0] and the other conditions are satisfied, incorrect read data is returned for the flash access.

2.2 Status

This errata will be fixed.

2.3 Workarounds

2.3.1 Workaround 1

Use FLASHBAR[6] to enable or disable the address speculation mechanisms of the flash controller. The default configuration (FLASHBAR[6] = 0) enables the address speculation. If FLASHBAR[6] equals 1, address speculation is disabled. Core performance may be degraded from 4% – 9%, depending heavily on application code.

NOTE

FLASHBAR[6] is user accessible via the movec instruction. FLASHBAR[6] always reads back as 0.

2.3.2 Workaround 2

Construct the device memory map so the flash and SRAM spaces are disjoint within the modulo-(flash_size) addresses. This allows for flash speculation to remain enabled. If this approach is selected, it would typically require the upper portion of the flash memory be unused and the SRAM be mapped to this unused flash space.

Consider an example where the flash memory size is 256 Kbytes and the on-chip SRAM size is 32 Kbytes. If 224 Kbytes or less of flash are used, then the SRAM can be based at the upper 32 Kbytes (within the modulo-256 Kbyte address) of the flash address space:

```
Flash: size = 0x40000, base = 0x0000_0000

RAM: size = 0x08000, base = 0x8003_8000 = RAM_BASE+(256-32) Kbytes
```

where the flash and SRAM base addresses are unique BA[31:16].

In summary, this approach can be applied if the combined size of the used flash and used SRAM is 256 Kbytes or less, with the flash contents justified to the lower address range and the SRAM contents justified to the upper address range.

2.3.3 Workaround 3

Separate the contents of the SRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR and RAMBAR to restrict accesses. This allows flash address speculation to remain enabled. For example, if the flash contains only instructions and the SRAM contains only operands (all data), the appropriate address space mask fields are specified and speculation can remain enabled.

3 Document Revision History

Table 2 provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Substantive Change(s)
Jun 2006, Rev 0	Initial release.
Nov 2006, Rev 1	• Reformatted document. • Added Section 2, “Internal Flash Speculation Address Qualification Incomplete.” Updated Table 1. • Text changes for grammar and punctuation.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-0047, Japan
0120 191014 or +81 3 3440 3569
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MCF52235DE
Rev. 1
11/2006