

Application note

Using DoCD debugger with Keil uVision2 tool ver 1.03

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1. OVERVIEW

The DoCD debugger fully supports Keil uVision2 AGDI interface to hardware debuggers. It allows Keil software users to work within uVision2 environments without switching between Keil compiler and external DoCD software. Everything - compilation, simulation, debugging - is under control of a single application. This document describes how to install and use DoCD debugger with programs written using Keil C/ASM tools.

2. SUPPLIED FILES

Delivered package contains a complete set of files, needed to run DoCD debugger inside uVision2 interface. The following directories can be found inside package:

.\C51\BIN\	: Contains DoCD debugger DLL Target driver file
.\C51\INC\DCD\	: Contains DCD's 8051/80390 include files
.\C51\EXAMPLES\DoCD\	: Contains example C/ASM 8051 application
.\DATASHTS\DCD\	: Contains DCD's 8051/80390 related PDF files
.\ UV2 \	: Contains DCD's 8051/80390 uVision2 database

This package is delivered to all existing DCD's customers. You may also order the DoCD FPGA evaluation kit by emailing us directly info@dcd.pl, and receive complete debug system to start working with our 8051/80390 IP Cores.

3. INSTALLATION

Manual installation of <u>DoCD target driver</u> is no longer required, because package is delivered as executable program, and all steps are performed automatically by setup program. The description provided below is left for informational purposes.

In order to use DoCD target driver follow the steps:

- Install µVision2 and the C51 Compiler on your machine. You may try to use evaluation version of 8051 Keil software at http://www.keil.com/demo/eval/c51.htm
- Unzip the file <u>DoCDTarget.zip</u> (if delivered) inside the <u><Keil install path>\</u> folder. The new files should appear inside <u><Keil install path>\C51\BIN</u>, <u><Keil install path>\UV2</u> and <u><Keil install path>\UV2</u> and <u><Keil install path>\UV2</u>
- Add the following lines to the TOOLS.INI file located inside <<u>Keil install path>\</u>folder:
 - section [C51]: TDRV0=BIN\DCD_DoCD.DLL ("DoCD 8051 Target Driver") Note: if TDRV0 is already in use, then use the next free digit, for example TDRV1
 - section [UV2]: CDB0=UV2\DCD.CDB("Digital Core Design") Note: if CDB0 is already in use, then use the next free digit, for example CDB1

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4. **PREPARING TO WORK WITH UVISION2 INTERFACE**

In order to run your application inside hardware using DoCD target driver follow the steps:

- Run μVision2. Select 'Project Open Project', the Select Project dialog comes up. Select the 'DoCD.uv2' project. It can be found normally in the folder - <u><Keil install</u> <u>path>\C51\EXAMPLES\DoCD</u>.
- Select 'Options for Target Devices'. From the 'Database' list-box, select "Digital Core Design" which is our devices database. Select required microcontroller type you actually have. If everything is right, then the dialog should look like this:

Options for Target 'DoCD'			
Device Target Output Listing C51 Database: Digital Core Design Generic CPU Data B Vendor: Digital Core Digital Core Design Device: DP8051 Family: MCS-51	A51 BL51 Locate BL51 Misc Debug Utilities		
 Digital Core Design DP80390 DP80390CPU DP80390CPU DP8051 DP8051 DP8051XP DP8051XP DR80390 DR80390CPU DR80390CPU DR80390CPU DR8051 DR8051 DR8051 DR8051XP DR8051XP DR8051XP 	 8051 based Pipelined High Performance Microcontroller IP Core with DoCD - DCD on-Chip Debugger. It is available for FPGA and ASIC usages as fully synchronous design with single clock domain. Its architecture is 10 times faster compared to legacy 80C51. Main features and peripherals: up to 64 KB on-chip CODE, up to 64 KB off-chip CODE, 256 Bytes on-chip RAM, 16 MB XDATA, PMU - Power Management Unit, CODE/XDATA Wait State feature, 32 I/O lines, 2 Timers/Counters, 5 Interrupts/2 priority levels, UART, 		
OK Cancel Defaults			

- Select 'Rebuild all target files' to build the project.
- Select 'Options for Target Debug'. From the combo-box, select "DoCD 8051 Target Driver" which is our DoCD driver. Make sure that the 'Use:' radio button is checked. If everything is right, then the dialog should look like this:

Options for Target 'DoCD'		
Device Target Output Listing C51 A51 BL51 Locate BL51 Misc Debug Utilities		
O Use Simulator Settings	O Use: DoCD 8051 Target Driver	
☑ Load Application at Startup ☑ Go till main()	🔽 Load Application at Startup 🛛 🔽 Go till main()	
Initialization File:	Initialization File:	
Restore Debug Session Settings	Restore Debug Session Settings	
🔽 Breakpoints 🔽 Toolbox	🔽 Breakpoints 🔽 Toolbox	
☑ Watchpoints & PA	Watchpoints	
Memory Display	Memory Display	
CPU DLL: Parameter:	Driver DLL: Parameter:	

• Select 'Settings' button. The 'Target Setup' dialog comes up.

Comm Port Settings	Cache Options
Port: Com 1	🔽 Cache Data
Clock Frequency Settings	Cache Xdata
Free: 20 (MHz)	Cache Code

Choose a COM port used by HAD board, enable at least CODE 'Caching Options'. Enter the actual clock frequency applied on-board to global CLK pin of 8051 IP Core. Allowed values are 1 MHz to 250 MHz. It means that DoCD will be working properly with CLK clock frequencies 2 times lower and 2 times higher than entered value.

• Close the both dialogs using 'OK' button. To discard all changes use 'Cancel' button.

5. DEBUGGING AN EXAMPLE PROJECT

This chapter describes how to use DoCD debugger with 8051 C/ASM application basing on example DoCD project. It is assumed that the installation and configuration steps had been performed. <u>You should also have DCD's 8051 core with Debug IP running inside some hardware prototype board equipped with FPGA or ASIC chip.</u>

Please follow the steps below:

 Run µVision2. Select 'Project – Open Project', the Select Project dialog comes up. Select the 'DoCD.uv2' project. It can be found normally in the folder - <u><Keil install</u> <u>path>\C51\EXAMPLES\DoCD</u>. The dialog should look like this:



 Select 'Rebuild all target files' to build the project. The build window shown above should report no warnings and errors.

🇇 🍱 🚈 👗 🐺 🖍 DoC				
Project Work Rebuild all target files				
🗁 😂 p.cp				

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http://www.DigitalCoreDesign.com http://www.dcd.pl • Start debugging by selecting 'Start/Stop Debug session'



• A warning dialog box may possibly be displayed after 5 seconds, if some communication problems with hardware board would be encountered.



In this case the cables should be checked for proper connection, and 'Retry' button pressed. 'Cancel' button closes debugging session.

• When hardware is properly configured, and program successfully uploaded/downloaded, then the debugger window should look similarly to picture below:



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• At this point debugging process is similar as in uVision2 simulator. The program can be run, halted, run step by step, breakpoints can be set/cleared. Variables can be watched, memory areas read/written/modified.

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6. NOTES

The following limitations are applied to the uVision2 debugger:

- 1. There are 4 independent complex hardware breakpoints available. There can be set using command line option or graphical boxes of uViison2 tool while debugging session is active:
 - at CODE space (PC value). Example command line: <u>BS main</u>- breakpoint at <u>main</u> address The only one breakpoint is active, regardless of number of set breakpoints (a red square displayed at the left side of C/ASM source editor).
 - at DATA space (READ, WRITE only). Example command line: <u>BS READ delay</u> - break when <u>delay</u> variable is being read
 - at SFR space (READ, WRITE only). Example command line: <u>BS WRITE DPH</u> - break when DPH SFR register is being written
 - at XDATA space (READ, WRITE only). Example command line: <u>BS WRITE x:0x34</u> - break when 0x34 address is being written

Please refer to uVision2 Debug Commands help file. Conditional breakpoints are not supported. To manage breakpoints select 'Debug | Breakpoints...' menu:



You should see the Breakpoints window. The selected breakpoint can be enabled, disabled, defined, or deleted.

Breakpoints	<u>? ×</u>
Current Breakpoints:	
 ✓ 00: (E) C:0x0A67, '\D0CD\44', ✓ 01: (E) C:0x0855, '\D0CD\65', ✓ 02: (A write D:0x83 len=1), 'dph', ✓ 03: (A read X:0x000034 len=1), 'x:0x34', 	
)
Expression:	Access
Count: 1	Size:
Command:	Dijects
Define Kill Selected Kill All	Close

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- 2. Code is automatically uploaded by uVision2 while debugging session is being started, and is assumed that CODE memory is writtable as SRAM. Please check DCD's 8051 IP Cores specification for more details about Program Memory writes.
- 3. In case of read only CODE memory (ROM, FLASH), user is responsible for proper image loading into physical chip holding CODE. <u>The CODE inside hardware memory must be identical with CODE used in uVision2 software</u>. In other case debugging won't work correctly.

7. **REFERENCES**

The DoCD uVision2 debugger package is delivered by DCD free of charge upon customer request. The customer should have DCD's 8051 IP Core equipped with DoCD on chip debugger, and HAD communication board. DoCD debug system is available at DCD web-site http://www.dcd.pl.

The Keil 8051 uVision2 tool suite is also required. It can be obtained from Keil GmbH at http://www.keil.com.

8. CONTACTS

For any questions or comments please contact DCD.

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