SECTION 8

Competitive Analysis of FFT Performances

8.1 Most Popular Digital Signal Processors

"The total Icycles of the DSP56156 can be reduced to about 44000 Icycles and the twiddle factors can be cut to N/2 with further optimization."

Currently a variety of DSPs are available from a dozen of semiconductor vendors. This section addresses floating-point DSPs first, because the FFT is one of their most important benchmarks. The architecture of floating-point DSPs is optimized for FFTs.

Fixed-point DSPs are also discussed because they have a higher performance-to-cost ratio than the floating-point DSPs, and are used more frequently in DSP applications such as digital audio, speech processing, telecommunication, automobile control, and home electronics. Since cost is a very sensitive issue in fixed-point DSPs, some useful features such as address mode, instruction type, number of input operands in each operation, and I/O capability can be offset with a reduction in silicon area to keep the cost as low as possible.

In general, the FFT performance on fixed-point DSPs is less than floating-point DSPs if the comparison is conducted on DSPs from the same vendor. But it is not surprising that a fixed-point DSP from one manu-

facturer may offer a higher performance than a floating-point DSP from a different manufacturer. After comparing existing DSPs, one may decide which is an optimal architecture for FFTs regarding speed and cost, where cost refers to required memory speed, memory size, and silicon area for special hardware that aides FFT calculation. It is impractical to base the decision on selling prices because they can be strongly influenced by sales strategies of different DSP vendors.

The following sections compare DSPs from Motorola, Texas Instruments, AT&T, and Analog Devices. There are other DSPs from new players that may have their merits, but they are not included in the following discussion due to their short time on the market.

8.2 Performance of FFTs on Digital Signal Processors

Digital signal processors can be divided into two categories; floating-point DSPs and fixed-point DSPs. As is well known, the fixed-point DSPs suffer saturation problems in calculations. To solve this problem, the programmer must scale down input data either at the front or in the middle of the calculation, which results in a shrunken signal-to-noise ratio or dynamic range. The floating-point DSPs use an extra data section to hold exponent information, consequently, the dynamic range is so large that the chance of

overflow is non-existent in most circumstances. Of course, one has to pay for this convenience by requiring wider data memory, a larger silicon area, and more power consumption.

8.2.1 FFTs on Floating-Point DSPs

Steps to implement various floating-point DSPs may differ depending on their conformance with the IEEE 754-1985 standard. In general, an IEEE floating-point DSP requires more computational steps to generate a normalized result than a proprietary implementation does. Although, the IEEE implementation may result in a bigger die design in achieving the same clock rate, it does, however, provide a standard interface to other microprocessors. In contrast, when proprietary formatted DSPs interface to other general purpose microprocessors, they require extra time to convert to the IEEE format. Motorola and Analog Devices are committed to the IEEE floating-point format. TI and AT&T use their own proprietary format.

Table 8-1 offers a fair comparison of complex FFTs on the different floating-point DSPs. Note that there are no constraints on the FFT algorithm. The FFT can be a Decimation in Time (DIT) or Decimation in Frequency (DIF), and can also be a radix two or radix four butterfly, as long as the algorithm can generate the best performance on a specified processor.

8.2.1.1 Complex FFT on Floating-Point DSPs

Table 8-1 1024-Point Complex FFT on Floating-Point DSPs

DSPs	96002[1]	AD21020[2]	TIC40[3]	TIC30[1]	AT&T32C[1]
Icycle (ns)	50	50	50	60	80
Algorithm	DIT	DIT	DIT	DIT	DIT
Radix	2	4	2	2	2
P Memory (word)	219	192	215	231	158
Data Memory (word)	4N	4N	4N	4N	2N
SIN/COS. table	3N/2	3N/2	N/2	N/2	N/2
Instruction length (bit)	32	48	32	32	32
SRAM for Zero Wait State (ns)	20	35	25	35	20

1. R.Meyer and K. Schwartz “FFT implementation on DSP-Chips-Theory and Practice” ICASSP, 1990.
2. Analog Devices, ADSP-21020 User’s Manual.
3. Texas Instruments, TMS320C4x User’s Guide.

NOTE: Icycle in Table 8-1 refers to **i**nstruction **cycle**. Minimum Icycle denotes the reciprocosity of the highest clock frequency available on the DSPs.

Table 8-1 shows that the Motorola DSP96002 performs the fastest 1024-point complex FFT. The Analog Devices' ADSP21020 performs almost as well as the DSP96002. The main factor that makes these two DSPs so fast in calculating the FFT is the special instruction "MPY||ADD||SUB". Supported by this instruction, the DSP96002 needs only four instruction cycles to perform one radix 2 butterfly, and the DSP21020 needs only fourteen instruction cycles to do one radix 4 butterfly. However, the DSP96002 has 2x512 data words on the chip and it features two on-chip DMA controllers. The on-chip memory and DMA controllers are extremely important features in implementing real-time data acquisition and control. The lack of peripherals and memory on the DSP21020 forces it into the position of competing with RISC chips. Although the DSP21020 requires lower cost SRAM for zero wait states interface, the program memory has to be 48-bits wide which negates the system cost benefits of using slow memory.

8.2.1.2 Real FFT on Floating-Point DSPs

Table 8-2 1024-Point Real Input FFT on Floating-Point DSPs

DSPs	96002[1]	TIC40[2]	TIC30[3]	AT&T32C[4]
Icycle (ns)	50	50	60	80
Total Icycles	11600	20396	31317	26300
Total Time (ms)	0.58	1.01984	1.879	2.106

1. See RFFT96T.asm on the Motorola DSP Bulletin Board (Dr. BuB).
2. Texas Instruments, TMSC4x User's Guide
3. Texas Instruments, Digital Signal Processing Applications with the TMS320 Family.
4. AT&T DSP32C User's Manual.

8.2.2 FFT on Fixed-Point DSPs

As mentioned previously, scaling must be performed on the fixed-point DSPs to prevent overflow in the intermediate stage of calculation. The following benchmarks, either complex or real FFT, assume that each input data has been divided by the number of the FFT.

8.2.2.1 Complex Input FFT

Table 8-3 1024-Point Complex FFT on Fixed-Point DSPs

DSPs	56001/2[1]	AD2100A[2]	TIC25[3]	TIC50[3]	56156[4]
Icycle (ns)	60/50	80	80	35	33
Algorithm	DIT	DIT	DIT	DIT	DIT
Radix	2	4	2	2	2
P Memory (word)	234	222			158
Data Memory (word)	4N	4N	2N	2N	4N
SIN/COS table	N/2	3N/2	5N/4	5N/4	N
Instruction length (bit)	24	24	16	16	16
Total Icycles	29949	34625	113487	82761	46373
Total Time (ms)	1.79694/ 1.49745	2.77	9.079	2.8967	1.53031

1. See CFFT56.asm on the Motorola DSP Bulletin Board (Dr. BuB).
2. R.Meyer and K. Schwartz “FFT Implementation on DSP Chips — Theory and Practice” ICASSP, 1990.
3. Texas Instruments TMS320 DSP Family Benchmarks.
4. See CFFT156.asm on the Motorola DSP Bulletin Board (Dr. BuB).

As shown in Table 8-3, the Motorola DSP56001/2 has a minimum icycle time and uses only N/2 locations for both real and imaginary twiddle factors. The total Icycles of the DSP56156 can be reduced to about 44000 Icycles and the twiddle factors can be cut to N/2 with further optimization.

8.2.2.2 Real Input FFT

Table 8-4 1024-Point Real Input FFT on Fixed-Point DSPs

DSPs	56002[1]	TIC25[2]	TIC50[2]
Icycle (ns)	50	80	35
Total Icycles	17443	56286	48055
Total Time (ms)	0.87215	4.50288	1.6819

1. See RFFT56T.asm on the Motorola DSP Bulletin Board (Dr. BuB).
2. Texas Instruments TMS320 DSP Family Benchmarks.