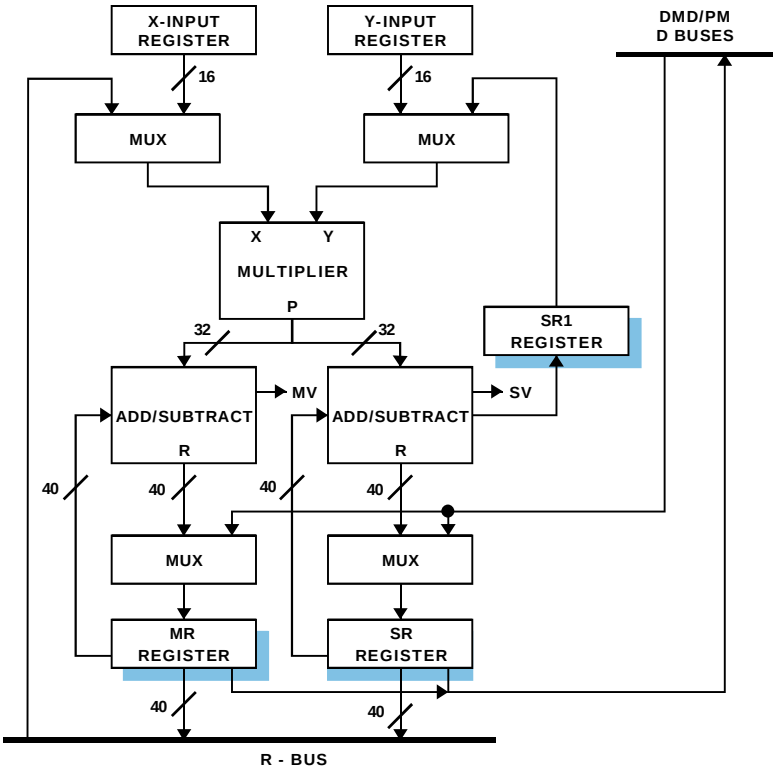

Figure 2-13. Multiplier Block Diagram

These registers each consist of smaller 16-bit registers: MR0, MR1, MR2, SR0, SR1, and SR2. For more information on these registers, see Figure 2-12 on page 2-28.

The adder/subtracters are greater than 32 bits to allow for intermediate overflow in a series of multiply/accumulate operations. A multiply overflow (MV or SV) status bit is set when an accumulator has overflowed beyond the 32-bit boundary—when there are significant (non-sign) bits in the top nine bits of the MR or SR registers (based on two's complement arithmetic).